

# BUK98150-55A

N-channel TrenchMOS logic level FET

Rev. 04 — 11 June 2007

Product data sheet

## 1. Product profile

### 1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package using NXP General Purpose Automotive (GPA) TrenchMOS technology.

### 1.2 Features

- Very low on-state resistance
- 150 °C rated
- Q101 compliant
- Logic level compatible

### 1.3 Applications

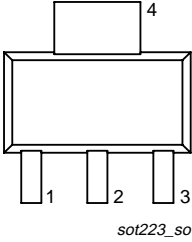
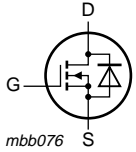
- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V and 24 V loads

### 1.4 Quick reference data

- $E_{DS(AL)S} \leq 22$  mJ
- $I_D \leq 5.5$  A
- $R_{DS(on)} = 128$  m $\Omega$  (typ)
- $P_{tot} \leq 8$  W

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	 <p style="text-align: center;">SOT223 (SC-73)</p>	 <p style="text-align: center;">mbb076</p>
2	drain (D)		
3	source (S)		
4	soldering point; connected to drain (D)		

### 3. Ordering information

**Table 2: Ordering information**

Type number	Package		Version
	Name	Description	
BUK98150-55A	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

### 4. Limiting values

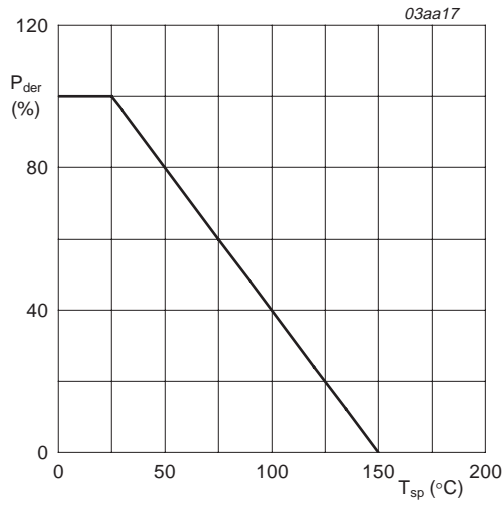
**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	55	V
$V_{DGR}$	drain-gate voltage (DC)	$R_{GS} = 20 \text{ k}\Omega$	-	55	V
$V_{GS}$	gate-source voltage		-	$\pm 15$	V
$I_D$	drain current	$T_{sp} = 25 \text{ }^\circ\text{C}$ ; $V_{GS} = 5 \text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	5.5	A
		$T_{sp} = 100 \text{ }^\circ\text{C}$ ; $V_{GS} = 5 \text{ V}$ ; see <a href="#">Figure 2</a>	-	3	A
$I_{DM}$	peak drain current	$T_{sp} = 25 \text{ }^\circ\text{C}$ ; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	22	A
$P_{tot}$	total power dissipation	$T_{sp} = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 1</a>	-	8	W
$T_{stg}$	storage temperature		-55	+150	$^\circ\text{C}$
$T_j$	junction temperature		-55	+150	$^\circ\text{C}$
<b>Source-drain diode</b>					
$I_{DR}$	reverse drain current	$T_{sp} = 25 \text{ }^\circ\text{C}$	-	5.5	A
$I_{DRM}$	peak reverse drain current	$T_{sp} = 25 \text{ }^\circ\text{C}$ ; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$	-	22	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 5.5 \text{ A}$ ; $V_{DS} \leq 55 \text{ V}$ ; $R_{GS} = 50 \text{ }\Omega$ ; $V_{GS} = 5 \text{ V}$ ; starting at $T_j = 25 \text{ }^\circ\text{C}$	-	22	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		[1]	-	J

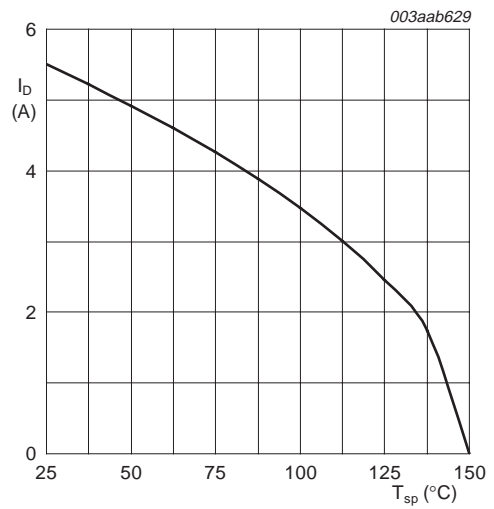
[1] Conditions:

- Value not quoted. Repetitive rating defined in [Figure 16](#).
- Single-pulse avalanche rating limited by  $T_{j(max)}$  of  $150 \text{ }^\circ\text{C}$ .
- Repetitive avalanche rating limited by an average junction temperature of  $145 \text{ }^\circ\text{C}$ .
- Refer to application note *AN10273* for further information.



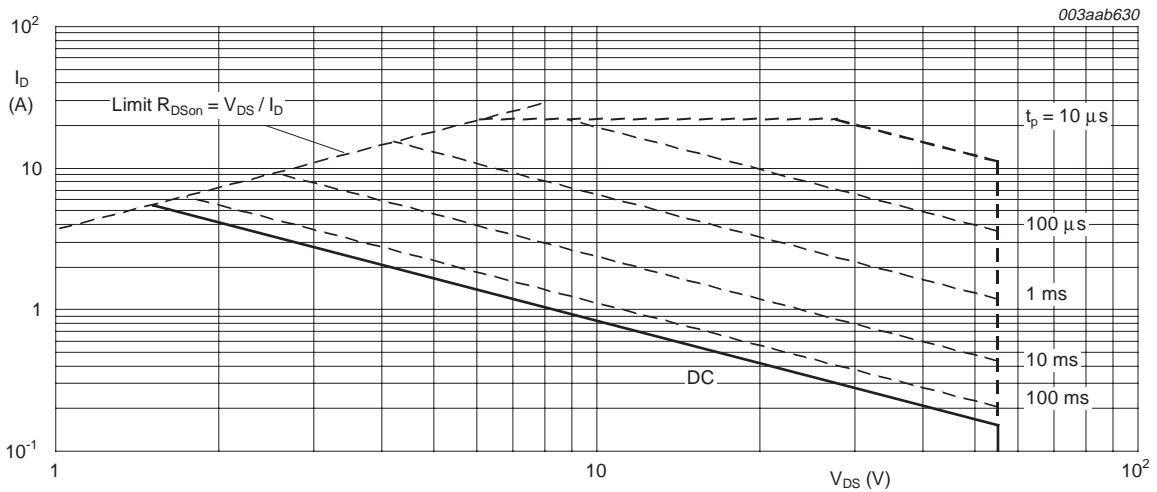
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of solder point temperature**



V<sub>GS</sub> ≥ 5 V

**Fig 2. Continuous drain current as a function of solder point temperature**



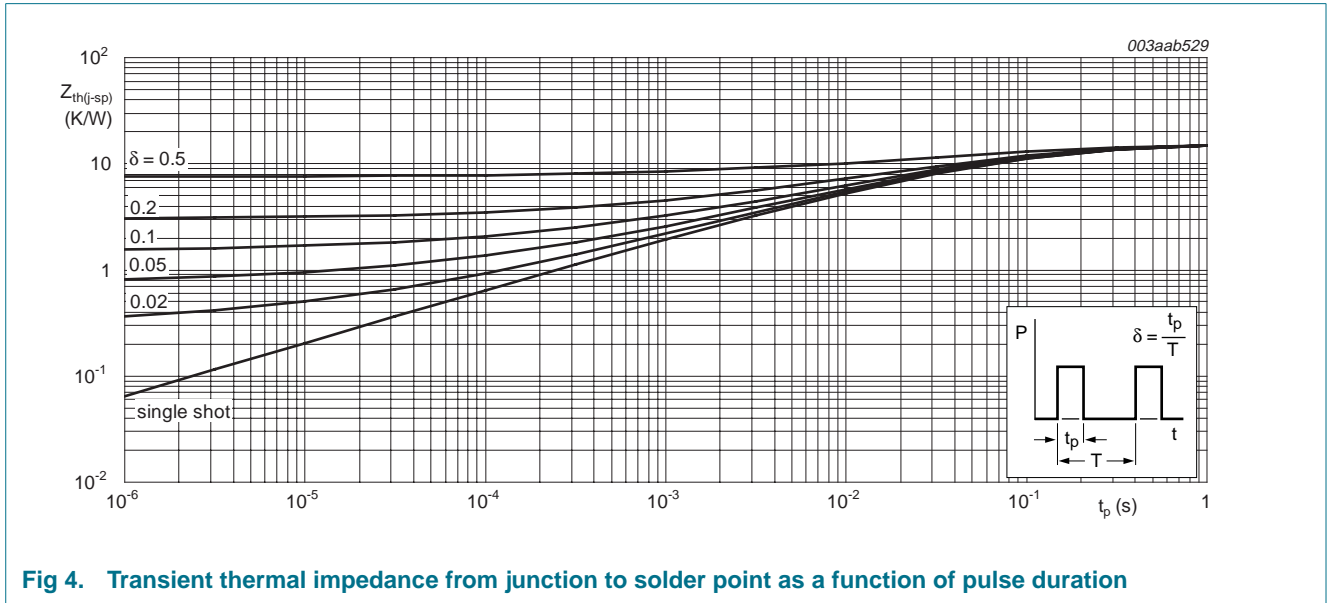
T<sub>sp</sub> = 25 °C; I<sub>DM</sub> is single pulse.

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

**5. Thermal characteristics**

**Table 4: Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	70	-	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	15	K/W

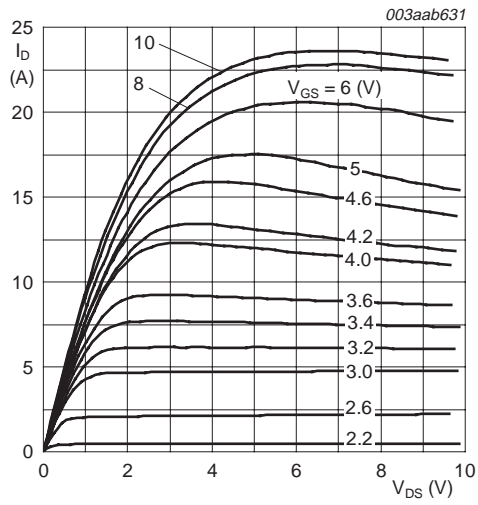


## 6. Characteristics

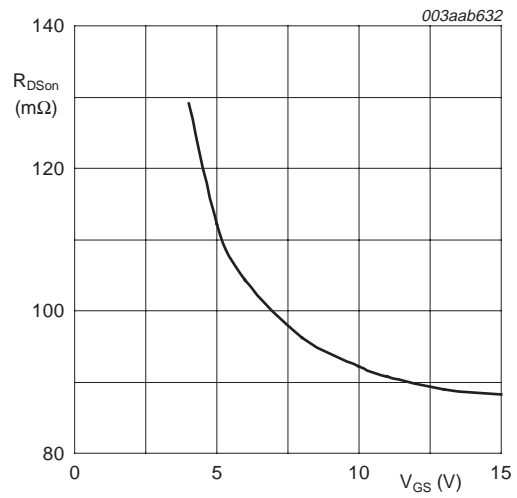
**Table 5: Characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

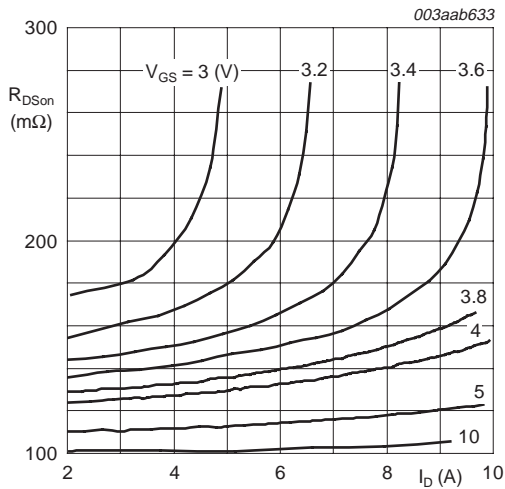
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	55	-	-	V
		$T_j = -55\text{ °C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$ ; see <a href="#">Figure 9</a>				
		$T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 150\text{ °C}$	0.6	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.3	V
$I_{DSS}$	drain leakage current	$V_{DS} = 55\ \text{V}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	-	0.05	10	$\mu\text{A}$
		$T_j = 150\text{ °C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 15\ \text{V}; V_{DS} = 0\ \text{V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\ \text{V}; I_D = 5\ \text{A}$ ; see <a href="#">Figure 7</a> and <a href="#">8</a>				
		$T_j = 25\text{ °C}$	-	128	150	m $\Omega$
		$T_j = 150\text{ °C}$	-	-	276	m $\Omega$
		$V_{GS} = 4.5\ \text{V}; I_D = 5\ \text{A}$	-	-	161	m $\Omega$
		$V_{GS} = 10\ \text{V}; I_D = 5\ \text{A}$	-	116	137	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 5\ \text{A}; V_{DD} = 44\ \text{V}; V_{GS} = 5\ \text{V}$ ; see <a href="#">Figure 14</a>	-	5.3	-	nC
$Q_{GS}$	gate-source charge		-	1	-	nC
$Q_{GD}$	gate-drain charge		-	2.8	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 25\ \text{V}; f = 1\ \text{MHz}$ ; see <a href="#">Figure 12</a>	-	240	320	pF
$C_{oss}$	output capacitance		-	53	64	pF
$C_{rss}$	reverse transfer capacitance		-	25	34	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\ \text{V}; R_L = 3.3\ \Omega$ ; $V_{GS} = 5\ \text{V}; R_G = 10\ \Omega$	-	8	-	ns
$t_r$	rise time		-	57	-	ns
$t_{d(off)}$	turn-off delay time		-	16	-	ns
$t_f$	fall time		-	13	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 5\ \text{A}; V_{GS} = 0\ \text{V}$ ; see <a href="#">Figure 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 5\ \text{A}; dI_S/dt = -100\ \text{A}/\mu\text{s}$ ;	-	24	-	ns
$Q_r$	recovered charge	$V_{GS} = -10\ \text{V}; V_R = 30\ \text{V}$	-	30	-	nC



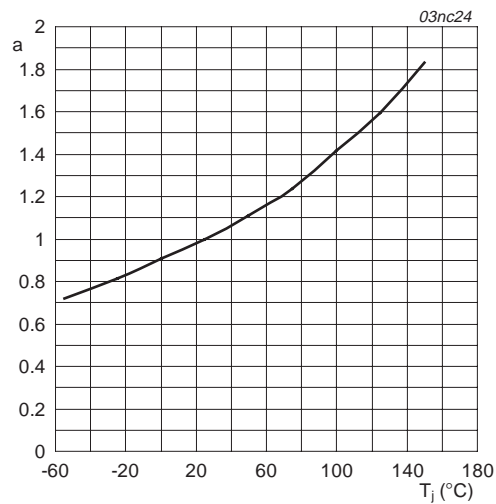
**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**

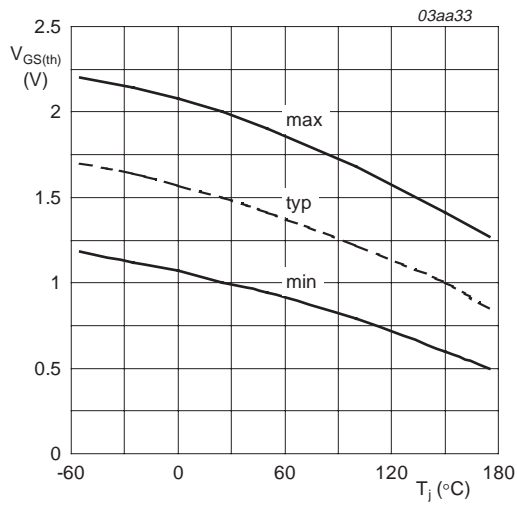


**Fig 7. Drain-source on-state resistance as a function of drain current; typical values**



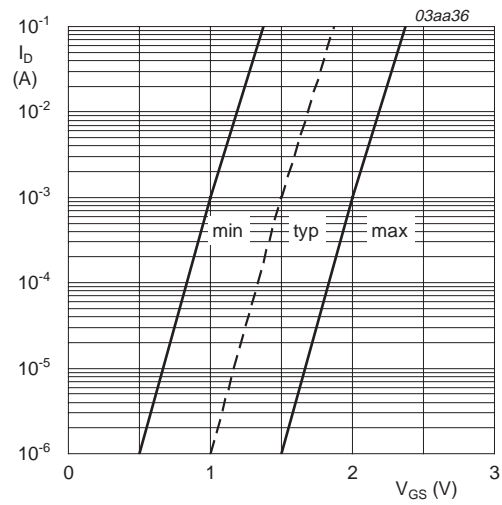
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature**



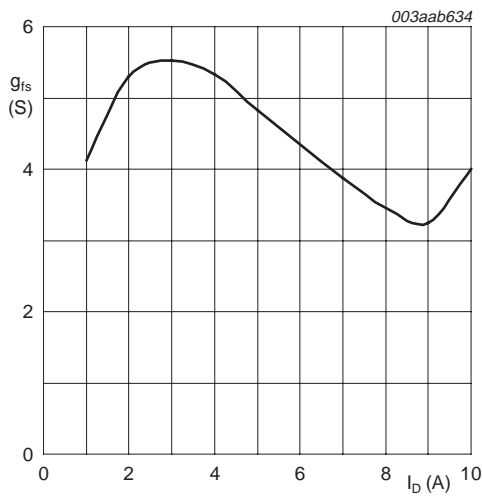
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig. 9. Gate-source threshold voltage as a function of junction temperature**



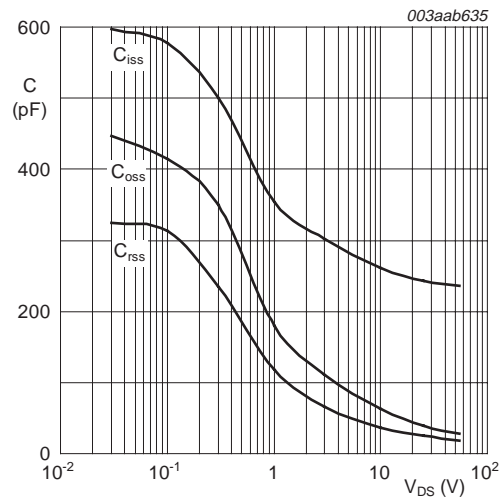
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**



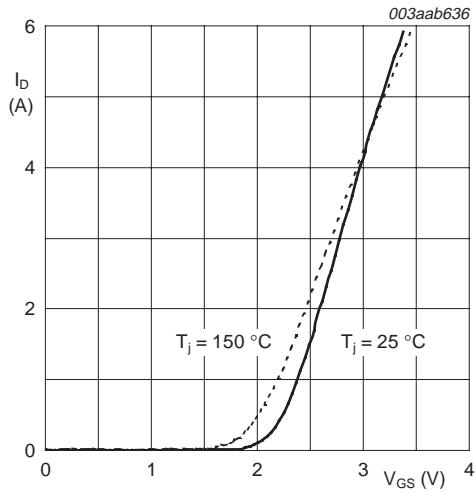
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

**Fig. 11. Forward transconductance as a function of drain current; typical values**

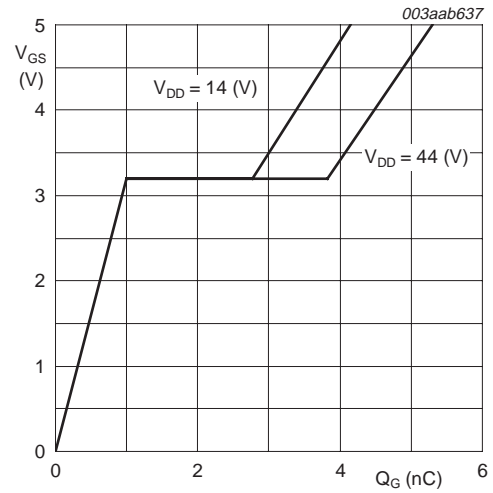


$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

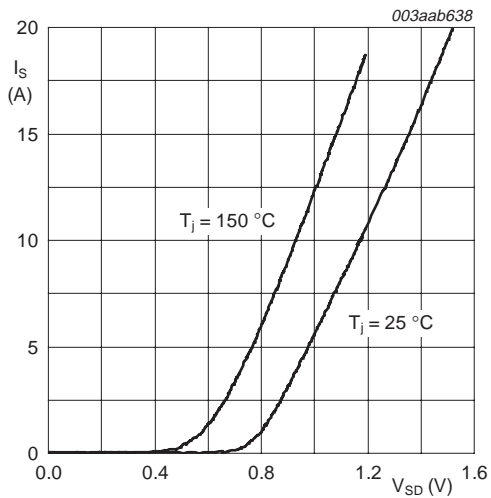
**Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



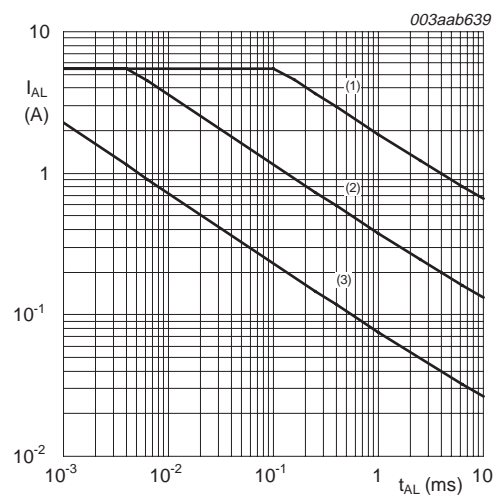
**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



**Fig 14. Gate-source voltage as a function of gate charge; typical values**



**Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**



See [Table note 1](#) of [Table 3](#) Limiting values.

- (1) Single-pulse;  $T_j = 25\text{ }^\circ\text{C}$ .
- (2) Single-pulse;  $T_j = 125\text{ }^\circ\text{C}$ .
- (3) Repetitive.

**Fig 16. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time**



**7. Package outline**

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223

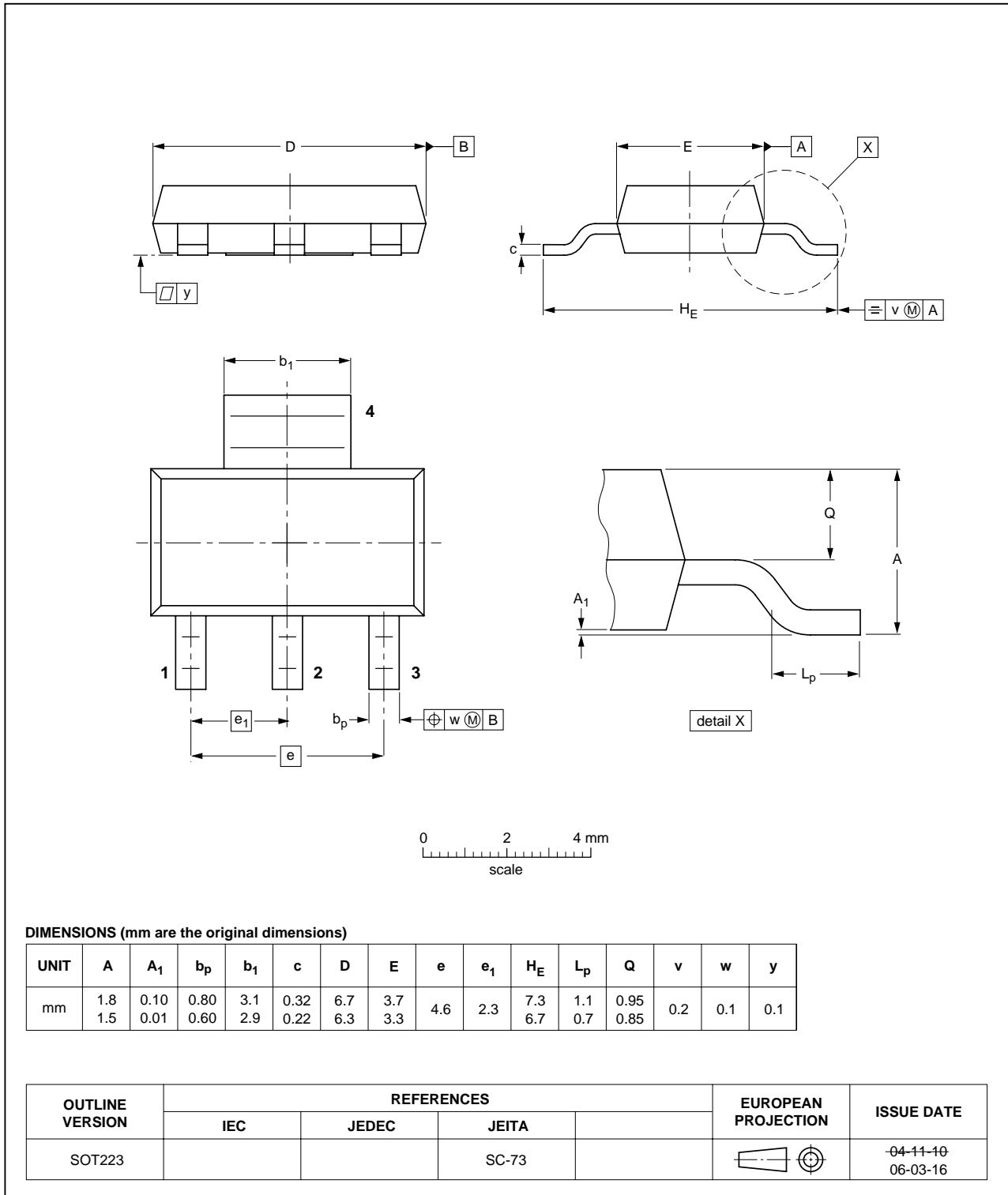
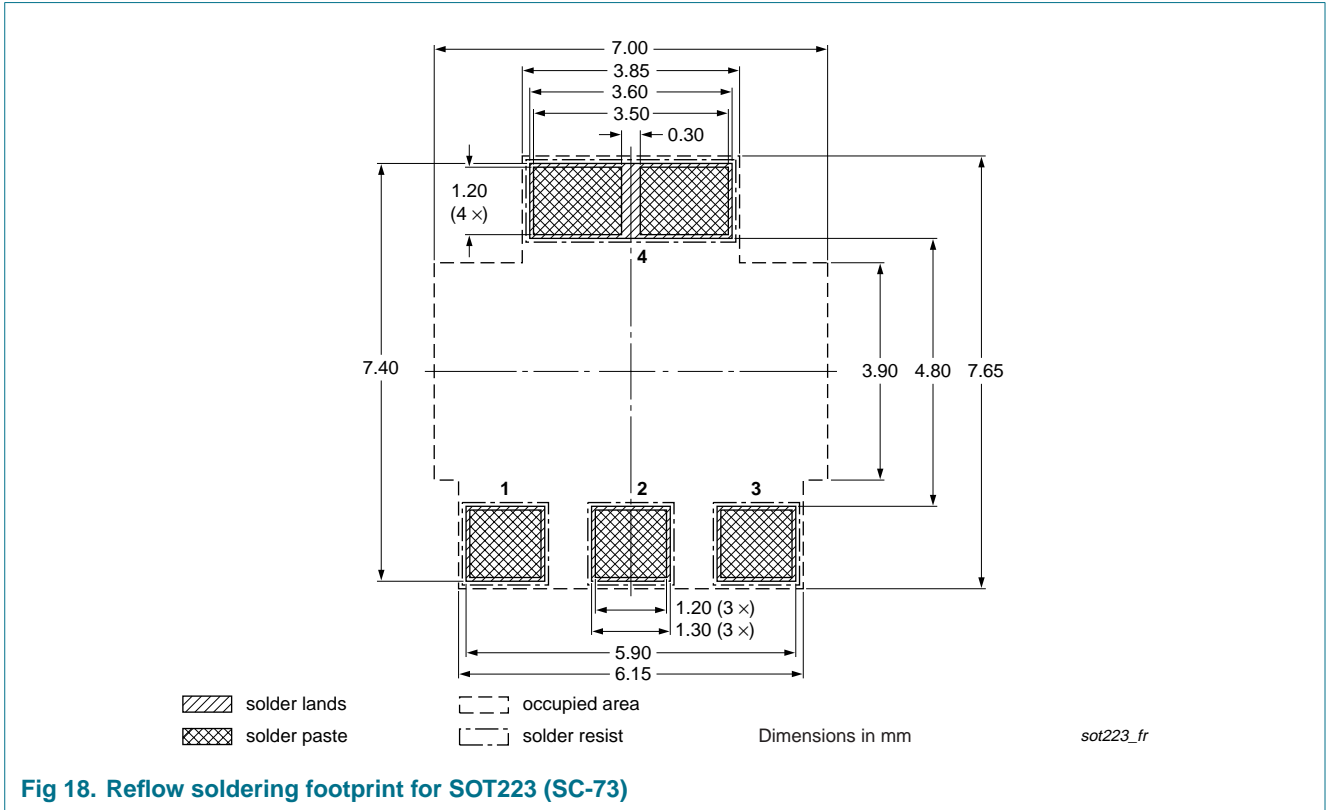


Fig 17. Package outline SOT223 (SC-73)

**8. Soldering**



**Fig 18. Reflow soldering footprint for SOT223 (SC-73)**

## 9. Revision history

**Table 6. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK98150-55A_4	20070611	Product data sheet	-	BUK98150-55A_3
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 5</a>: IDSS drain leakage current condition changed from <math>T_j = 175\text{ °C}</math> to <math>T_j = 150\text{ °C}</math> due to typing error.</li> </ul>			
BUK98150-55A_3	20061124	Product data sheet	-	BUK98150-55A_2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Table 5: changed Typ and Max <math>C_{OSS}</math> output capacitance values from 40 pF to 53 pF and 48 pF to 64 pF respectively because of typing error.</li> </ul>			
BUK98150-55A_2	20020325	Product data sheet	-	BUK98150-55A_1
Modifications:	<ul style="list-style-type: none"> <li>• Table 3: Gate-source voltage maximum increased from <math>\pm 10\text{ V}</math> to <math>\pm 15\text{ V}</math></li> <li>• Table 4: <math>R_{th(j-sp)}</math> maximum decreased from 20 K/W to 15 K/W</li> <li>• Table 5: Switching speed measurements updated</li> <li>• Section 1.4 and Table 3: Total power dissipation, peak drain current, peak reverse drain current, and non-repetitive avalanche energy values updated.</li> </ul>			
BUK98150-55A_1	20001003	Product data sheet	-	-

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### 10.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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